Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.

**PAD FUNCTIONS:**

1. **OUTPUT**
2. **ADJ**
3. **OUTPUT**
4. **INPUT**
5. **OUTPUT**

**.071”**

**1**

**2**

**5**

**3**

**4**

**.110”**

**Top Material: Al**

**Backside Material: TiNiAg**

**Bond Pad Size: .004 x .004” min.**

**Backside Potential: VOUT**

**Mask Ref:**

**APPROVED BY: DK DIE SIZE .071” X .110” DATE: 10/13/21**

**MFG: NATIONAL THICKNESS .013” P/N: LT1086-ADJ**

**DG 10.1.2**

#### Rev B, 7/1